Vectorizing Database Column Scans with Complex Predicates

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   - Overview
   - General Scan Algorithm
   - Optimizations

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4. Conclusion and Outlook
Memory has become large enough to contain all data.
In-memory Architecture

- Keeping data in memory allows faster access to data, overcomes disk latency.
- Backup is kept on storage.
Disruptive change in RDBMS industry

- Rise of In-Memory Databases (IMDBs).
- Anticipated by research 10+ years ago.
- All major DB vendors are working on it.
- SAP leading with HANA as platform for all new apps.
IMDBs often use Column-Orientation

Advantages of column-orientation:
- Columns compressed independently
- Leverages better compression
- Cache-friendly:
  - cache-line granularity
  - prefetching
- SIMD-friendly
“Dictionary” contains all distinct values (e.g. 100,000 entries)

- Valueld are integers from 0, 1, 2, 3, ..., 100000
- Max is N=100000 (number of distinct values), which needs 17 bits to represent (\(\lceil \log_2 N \rceil + 1 \))
- Idea: instead of 32-bits, use 17-bits fields to store each ValueID. We then call "17" the "Bit-case"
- Accessing “Value” needs decompression into 32-bits
Introduction, Context, and Motivation

Compression building blocks: Bit-Fields

Packed bit-fields

- Large number of integers, each with n number of bits

```
  F  E  D  C  B  A  9  8  7  6  5  4  3  2  1  0

128 4711 100000 42
```

32 bits
Packed bit-fields

- Large number of integers, each with n number of bits
- Example: 17-bit per entry:

32 different implementations for each n from 1 to 32.
For each query do a full-table scan, i.e.,
- Decompress required columns,
- Aggregate data according to predicate,
- Further processing.

Performance of unpacking is key for full-table scans!
We propose a framework for vectorized column scans with complex predicates.
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Different classes of predicates:
- Range predicates
- Vectorizable predicates
- In-list predicates
- Arbitrary predicates
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Different classes of predicates:
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Different output formats:
- Bit vectors
- Index vectors
- Unpacked data
Vectorized Scan Framework: General Scan Algorithm

- Common scheme for all predicates and output formats
- Extensible with templates
- Vectorized processing of 8 values at a time (or more)
- Manual optimizations of all paths and all bit cases
Vectorized Scan Framework: General Scan Algorithm

- **shuffle**
- **clean**
- **align**
- **buffer**

- **compare**
- **extract bits**
- **extract indices**
- **store**

- **«vectorized code»**
- **«arbitrary code»**

- Next DB operator

- Byte level shuffle

- SHUFFLE

- Byte #
Vectorized Scan Framework: General Scan Algorithm

- shuffle
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- «vectorized code»
- «arbitrary code»

Byte #

... 0F 0E 0D 0C 0B 0A 09 08 07 06 05 04 03 02 01 00 ...

- V4
- V3
- V2
- V1

- 0xFFFFFFFF
- 0xFFFFFFFF
- 0xFFFFFFFF
- 0xFFFFFFFF

- Clean

- AND
Vectorized Scan Framework: General Scan Algorithm

- shuffle
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- «arbitrary code»
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Byte #

- V4
- V3
- V2
- V1

Vector-vector shift

- >> 4
- >> 0
- >> 4
- >> 0

Clean
Vectorized Scan Framework: General Scan Algorithm

Write to Buffer
Range predicates (can express all the equality predicates, i.e., $=, \neq, \geq, >, \leq, <$)
Vectorized Scan Framework: General Scan Algorithm

**COMPRESSED SEARCH (3, 30)**

<table>
<thead>
<tr>
<th>F</th>
<th>E</th>
<th>D</th>
<th>C</th>
<th>B</th>
<th>A</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>γ</td>
<td>x</td>
<td>42</td>
<td>4</td>
<td>27</td>
<td>32766</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **shuffle**
- **clean**
- **align**
- **buffer**

**«vectorized code»**

- **compare**
- **extract bits**
- **extract indices**
- **store**
- **next DB operator**

**Unpack**

Compare and mark hits in bit-vector

| 42 | 4 | 27 | 32766 |

Bit-Vector

0 1 1 0
Vectorized Scan Framework: General Scan Algorithm

shuffle

clean

align

buffer

«vectorized code»

«arbitrary code»

extract bits

extract indices

store

next DB operator

COMPRESSED SEARCH (3, 30)

F E D C B A 9 8 7 6 5 4 3 2 1 0

... y x 42 4 27 32766

Unpack

Compare and store the index

2 1

Result Buffer
Many other predicates, including many arithmetic expressions on a single column, can easily be expressed using vector instructions. Example: In-list predicate.
Fall-back mechanism, where a block of codewords is unpacked as machine words into a buffer in cache, on which arbitrary predicates can be applied.
Vectorized Scan Framework: General Scan Algorithm

Store the different classes of results
Unpack a column for the subsequent database operator.
Optimizations can apply to a group of bit-cases. They can also be specific to one bit-case.
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Bit-case level optimizations are performance critical.
Vectorized Scan Framework: Optimizations

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- Optimizations allow to compare up to 32 values in parallel.
- For In-list predicates: "Permute" and "AvoidGather" are necessary to achieve optimal performance.
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Example: Scan algorithm for In-list predicate.
Vectorized Scan Framework: Optimizations

Search the values that are marked in a bitvector:

1. **UNPACK**
2. If corresponding bit is set
3. Mark bit in result bitvector

```
COMPRESSEDSEARCH(bitvec)
```

|   |   |   |   | A | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ... | y | x | 42 | 4 | 27 | 32766 |
Vectorized Scan Framework: Optimizations

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```
COMPRESSEDSEARCH(bitvec)

F  E  D  C  B  A  9  8  7  6  5  4  3  2  1  0

... y x 42  4  27 32766
```

Predicate Bit-Vector

```
... 0 1 1 0 0 1 1 1 0 1 1 0
```

4  0
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**COMPRESSED SEARCH (bitvec)**

- Decompress
- Is bit 4 set?
- Set bit for 3rd value
Vectorized Scan Framework: Optimizations

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Vectorized Scan Framework: Optimizations

COMPRESSED SEARCH (bitvec)

F E D C B A 9 8 7 6 5 4 3 2 1 0

... y x 42 4 27 32766

Decompress

42 4 27 32766

Predicate Bit-Vector

... 0 1 1 0 0 1 1 1 0 1 1 0

Is bit 4 set?

Set bit for 3rd value

Result Bit-Vector

0 1 1 0

4 0

How to implement these steps in AVX2?
Two AVX2 instructions are key to achieve the parallelization of the Scan with in-list predicate algorithm:

- **Vector-vector shift instruction**: The new vector-vector shift instructions allows shifting each word of the AVX register with an independant value. We use it to convert the values into words where only the bit at the index equal to the value is set to 1.

- **Gather instruction**: The new gather instructions loads elements from memory based on a base address and offsets for each data element. We use it to gather the different chunks of the predicate relevant to vectorized comparison.
Evaluation: Unpack Performance

- Bit cases have different performances due to different optimizations.
- Example: bit case 16 is trivially easy.
- AVX2-Scan is 30% faster than SIMD-Scan.
- Bit cases >16 are memory bound.
Lemire’s reimplementation of SIMD-Scan often matches our performance, but we found additional optimizations.

Li’s reimplementation needs 5 cycles/codeword.
Evaluation: Scan Performance

- Optimizations "Permute" and "AvoidGather" work very well for bitcases $\leq 8$.
- In these cases 4 times faster than Scalar.
- Bit cases $>21$ and $>26$ get penalties from L2 and L3 cache misses for the bit-vector predicate.
AVX2-Scan consistently 30% faster than SIMD-Scan.

Throughputs between 4 and 10 billion codewords per second with peaks of 17 billion.
Conclusion and Outlook

- Our scan framework, in particular the AVX2-Scan implementation, is an effective means to improve scan performance.
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Conclusion and Outlook

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- Intel has recently released the description of Intel AVX-512. Most notable additions:
  - 512 bit registers.
  - Mask registers.
  - Cross-lane shuffles.
  - Compress instruction.
  - Unsigned comparison.
Our scan framework, in particular the AVX2-Scan implementation, is an effective means to improve scan performance.

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It would be interesting to compare our approach with GPUs.