Evaluating SIMD Compiler-Intrinsics for Database Systems

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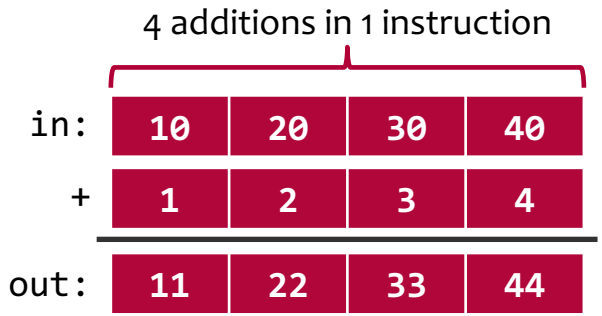
ADMS | 28.08.23

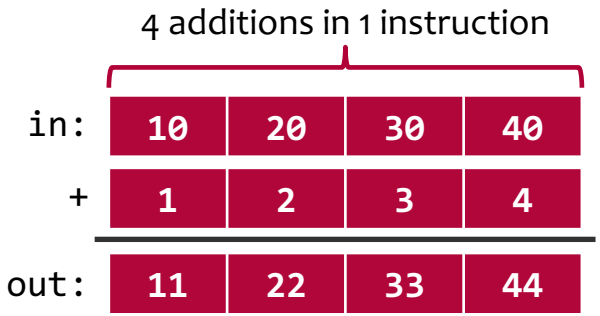
SIMD in a Nutshell

» Single Instruction Multiple Data (= SIMD)



SIMD in a Nutshell

- Single Instruction Multiple Data (= SIMD)
- Most common instruction sets
  - x86: SSE, AVX, AVX2, AVX512 (> 6k instructions)
  - ARM: Neon (> 4k instructions), SVE
  - PowerPC AltiVec, RISC-V V



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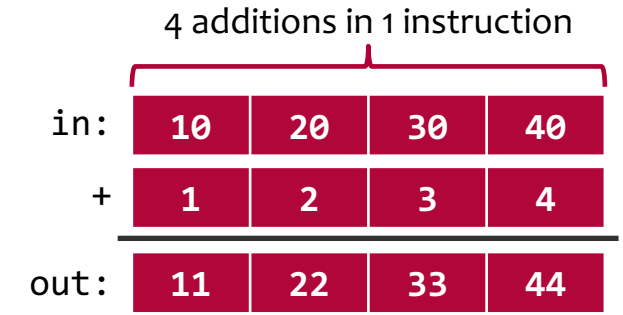

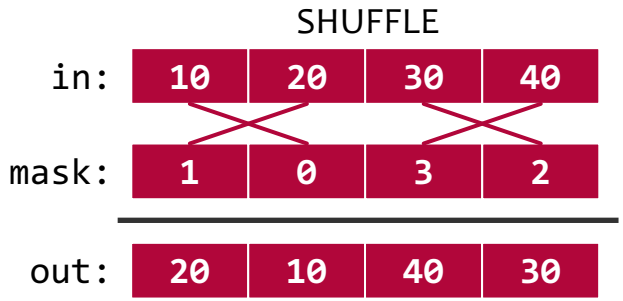

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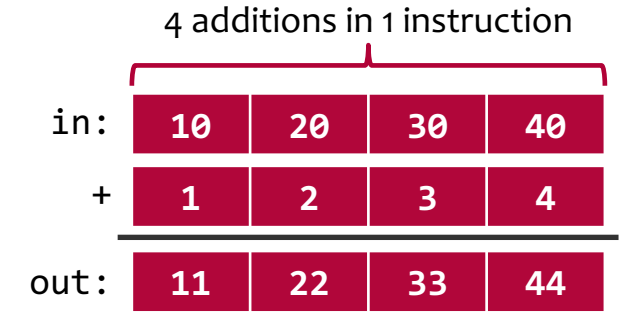
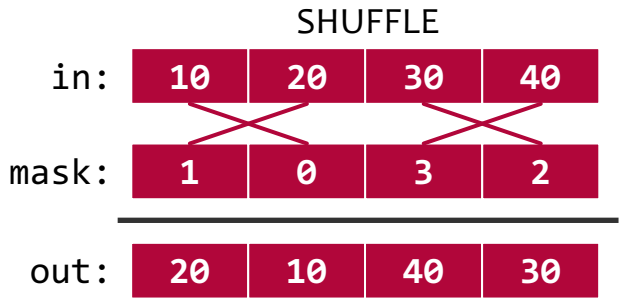
- Arithmetic, Logical, Shuffle, Shift, Load, Store, …
- Focus on x86 and Neon
  - x86: 128 – 512 Bit registers
  - Neon: 128 Bit registers





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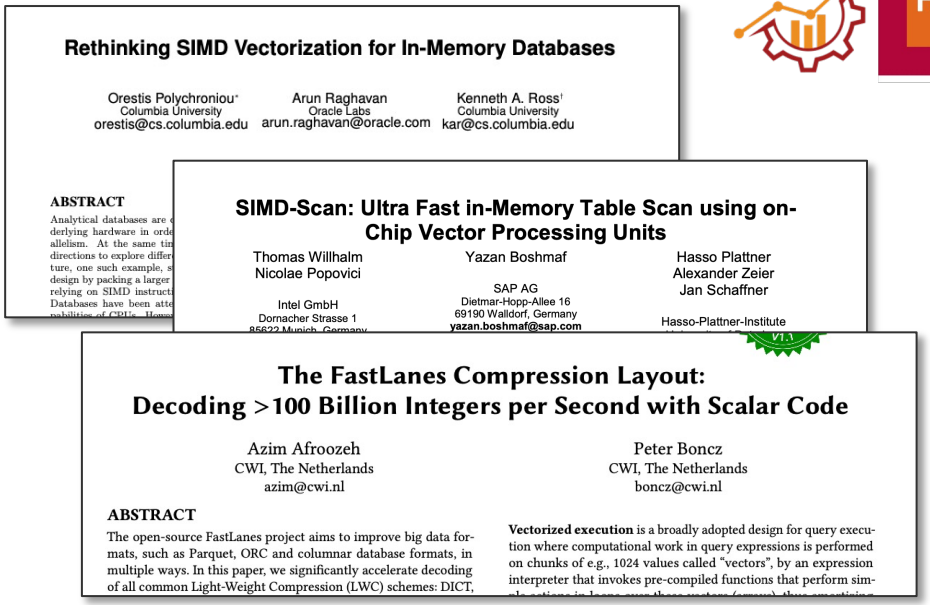

Rethinking SIMD Vectorization for In-Memory Databases

Orestis Polychroniou* Columbia University orestis@cs.columbia.edu
Arun Raghavan Oracle Labs arun.raghavan@oracle.com
Kenneth A. Ross† Columbia University kar@cs.columbia.edu

ABSTRACT

SIMD-Scan: Ultra Fast in-Memory Table Scan using on-Chip Vector Processing Units

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Nicolae Popovici
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Alexander Zeier
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The FastLanes Compression Layout:
Decoding >100 Billion Integers per Second with Scalar Code

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Peter Boncz
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ABSTRACT

The open-source FastLanes project aims to improve big data formats, such as Parquet, ORC and columnar database formats, in multiple ways. In this paper, we significantly accelerate decoding of all common Light-Weight Compression (LWC) schemes: DICT,

Vectorized execution is a broadly adopted design for query execution where computational work in query expressions is performed on chunks of e.g., 1024 values called "vectors", by an expression interpreter that invokes pre-compiled functions that perform sim-

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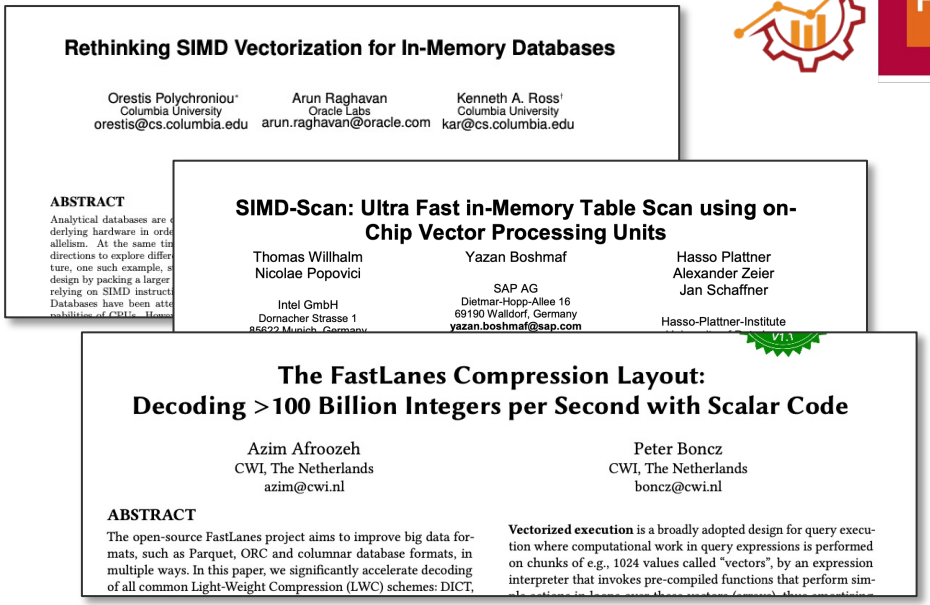

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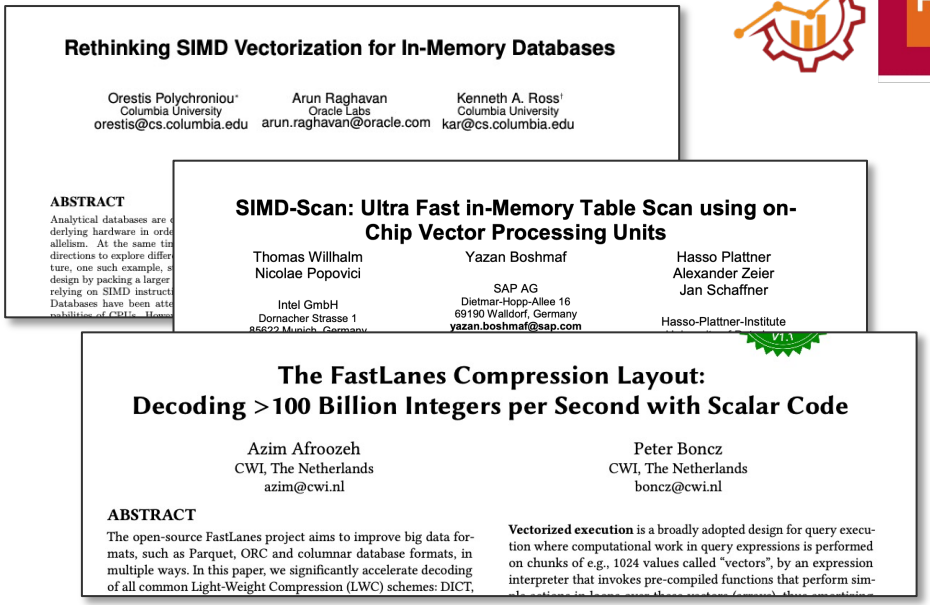

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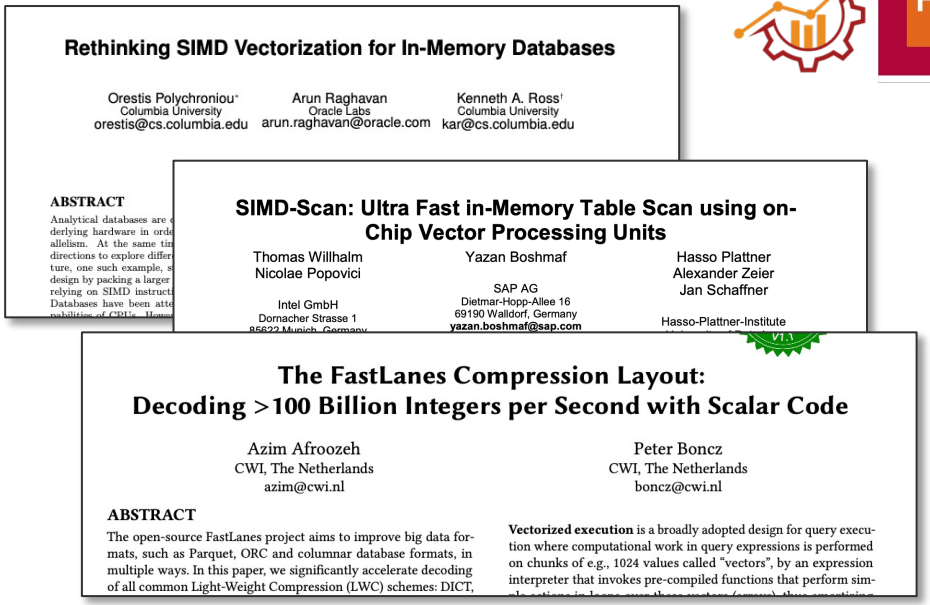

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What do these functions do?

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_mm512_srl_epi64()
vaddq_s32()
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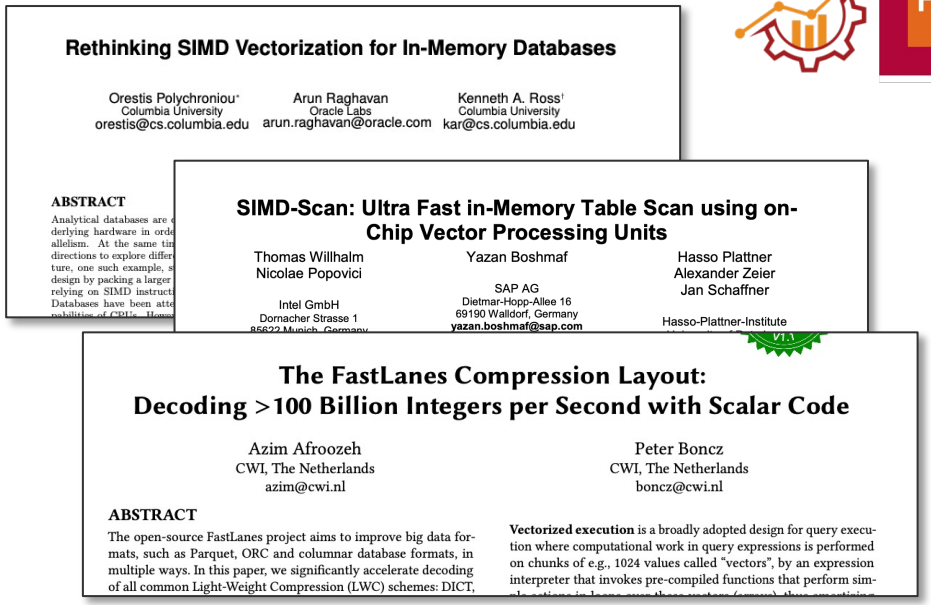

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Don't have AVX512?
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Don't have NEON?
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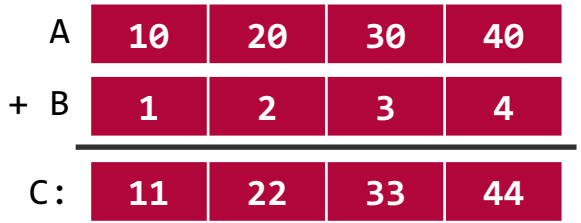
Abstractions on top of Abstractions

Add two 128-bit registers of 4x 32-bit integers



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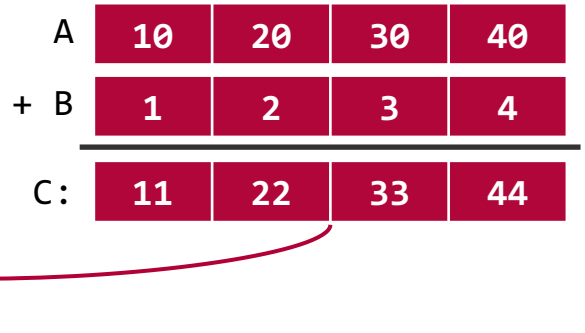

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vec C = A + B;
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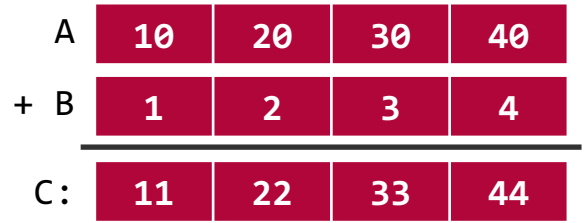

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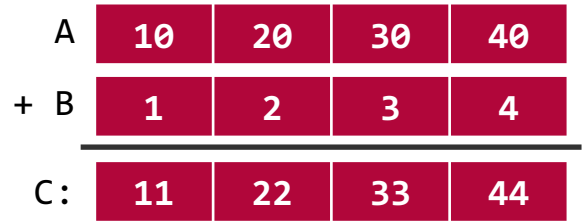

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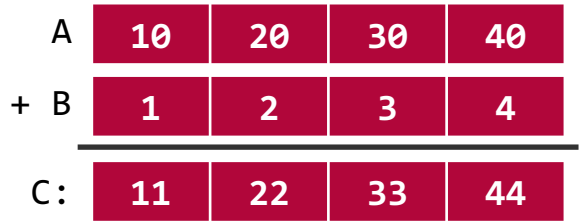

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Compiler representation

```
__attribute__((
   vector_size(N)));
```

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SIMD Types

16 Byte type in x86

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GCC/Clang's "vector" type

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int32x4_t vaddq_s32(int32x4_t __p0, int32x4_t __p1) {



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Platform- and type-dependent C API
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```
template <typename T>
using vec __attribute__((vector_size(16))) = T;

vec<T> foo(vec<T> a, vec<T> b) {
  // Do stuff
  vec<T> result = a + b;
  // ...
  return result;
}
```

Use compiler-intrinsics to structure code

Compiler-Intrinsics

- GCC/Clang have SIMD abstraction
  - via `__attribute__((vector_size(SIZE)))`
  - `SIZE` in bytes can be … / 8 / 16 / 32 / 64 /…

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25     // Write matching row ids to output.
26     *(UnalignedVec*)(output + num_matches) = compressed_rows;
27     num_matches += std::popcount(bitmask);
28   }
29   return num_matches;
30 }
```

Benchmarks

- M1: Apple Macbook Pro 14" M1 2021
- x86 Icelake: Intel Xeon Platinum 8352Y

- All experiments with:
  - Clang 15 (x86) and trunk Clang ~17 (ARM)
  - -O3, -march/-mtune=native

- Single-threaded
- Show relative speedup over scalar version

- Also other x86/ARM CPUs and GCC → see paper

Hash Bucket Lookup

» Vector comparison and conversion to scalar bitmask

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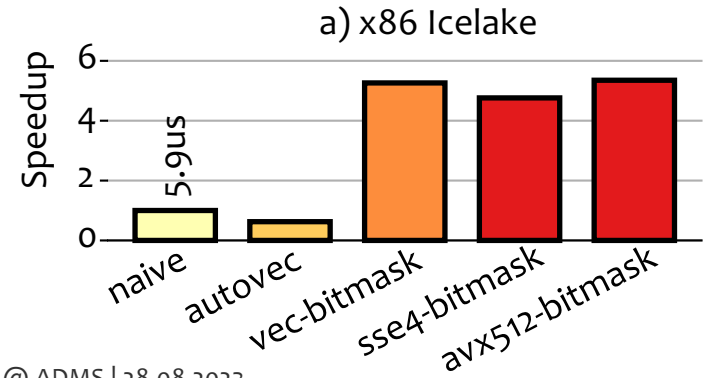

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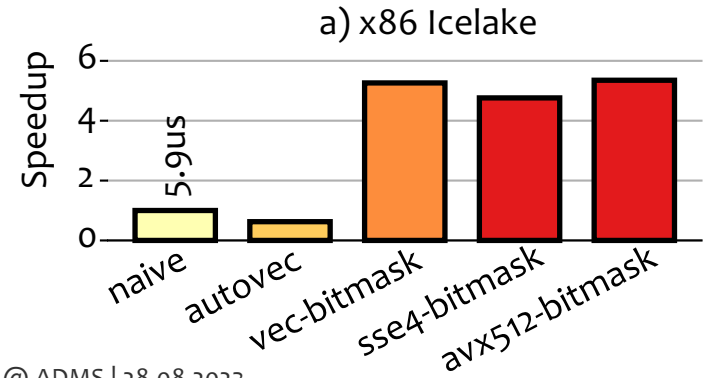

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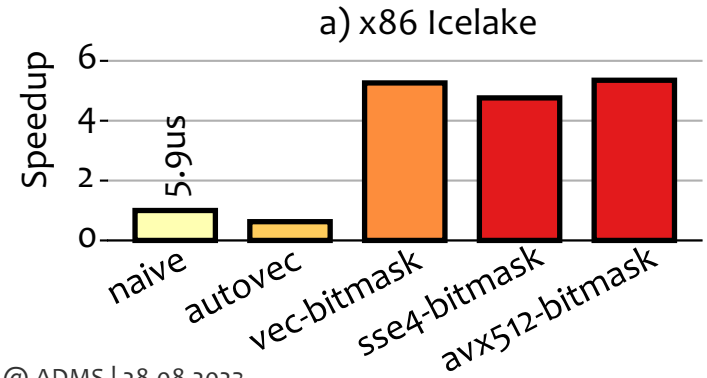

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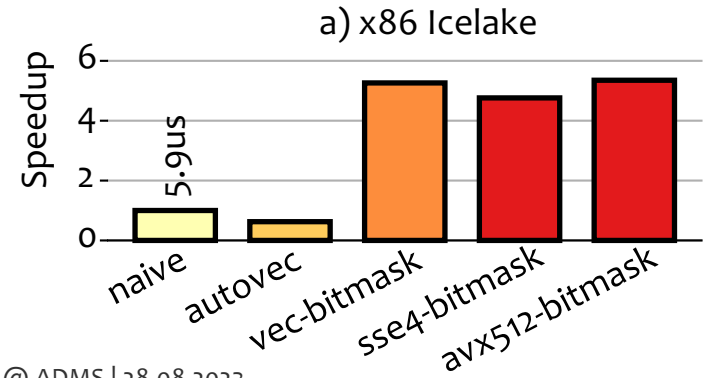
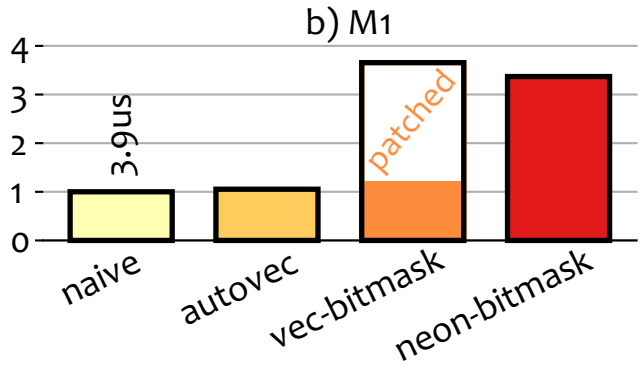
  - vec-bitmask does bitmask == 0 check before bitmask conversion





Bit-Packed Integer Decompression

» Unpack packed 9-Bit integers to 32 bits → shuffling + shifting + masking

SIMD-Scan: Ultra Fast in-Memory Table Scan using on-Chip Vector Processing Units
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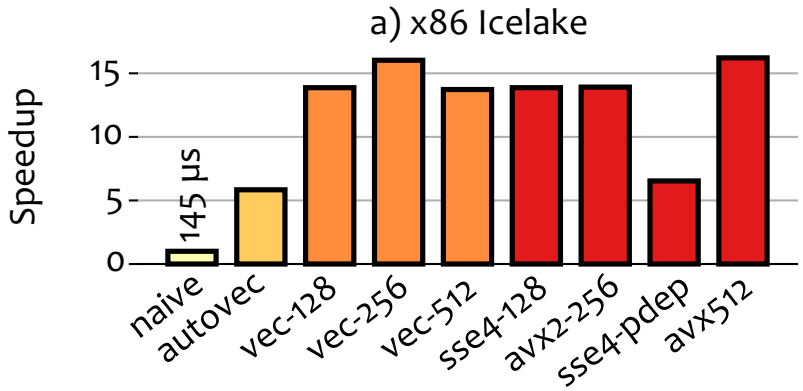

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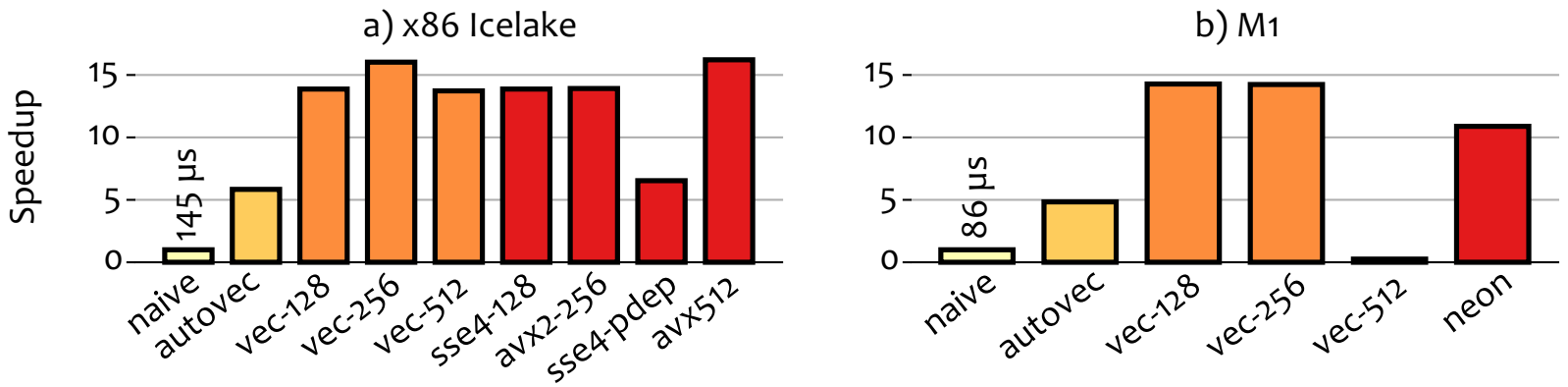

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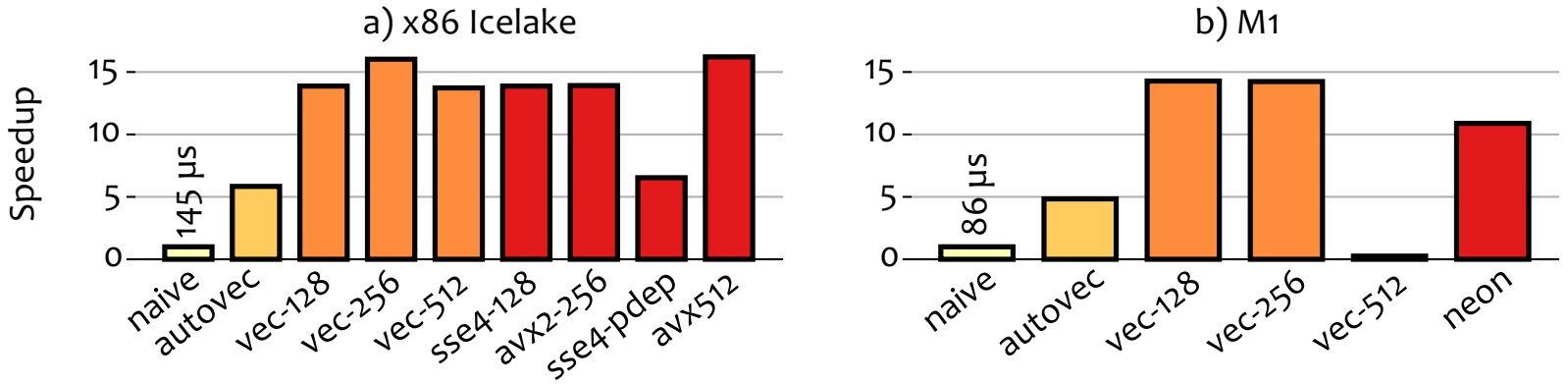
- Neon: *vec-512* not physically supported → bad performance



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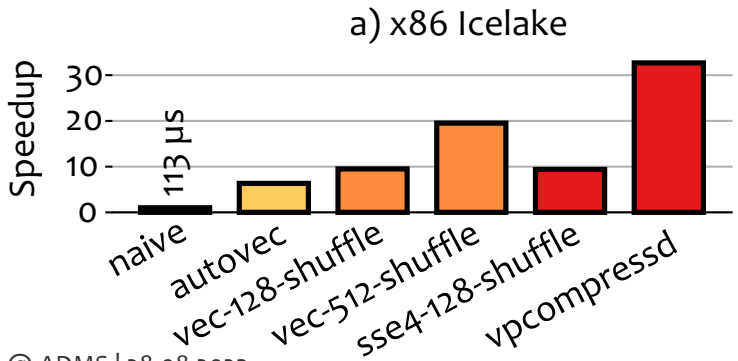

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- AVX512 `compresstore`
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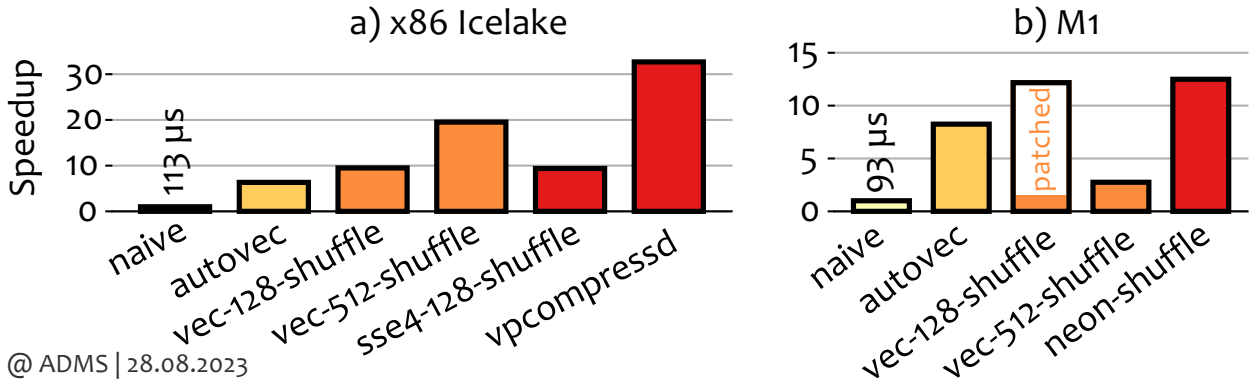
- NEON *vec-128*: Shuffling doesn't use TBL instruction
  - With our LLVM patch → equal to NEON performance



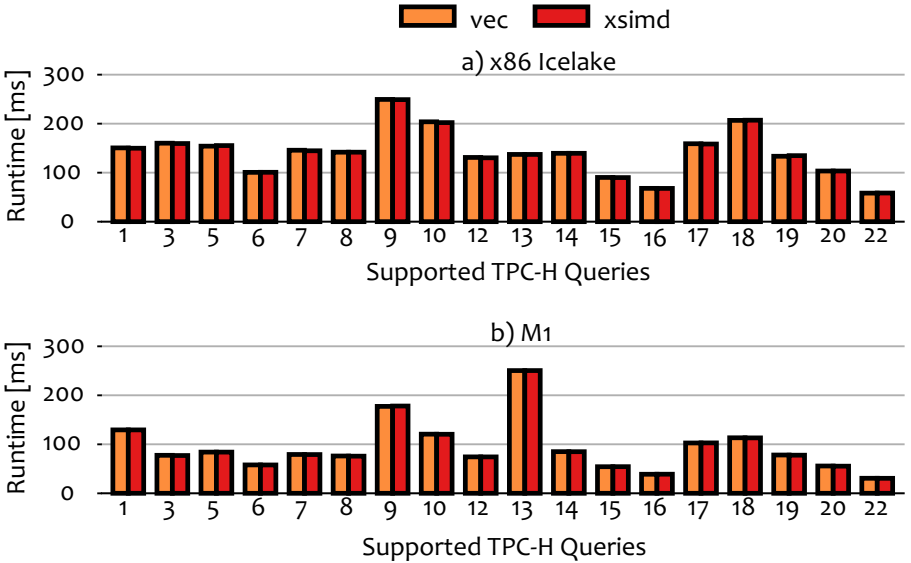
Compiler-Intrinsics in Velox

- Velox: Meta's new unified query engine

- Removed xSIMD dependency
- Use only compiler-intrinsics

- End-to-end TPC-H SF1
- x86 ⟶ 0.1% diff
- NEON ⟶ 0.13% diff

- Removed:
  - 54 platform-specific functions
  - Hundreds of lines of SIMD code



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» In 7/8 benchmarks + Velox: compiler-intrinsics ≈≈ platform-intrinsics

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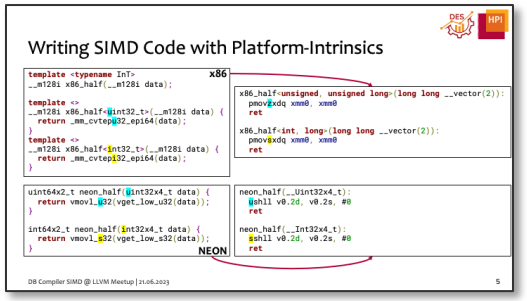
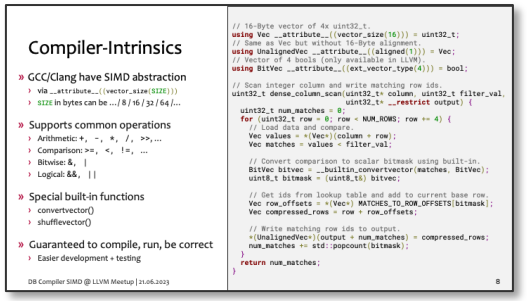
- Structure code around compiler-intrinsics
- Only localized platform-specific code
- Easier development + testing
  - Don't need AVX512 CPU for 512-bit vector code
- Potentially better/more optimizations
- Adapt SIMD code to own need, not dependency

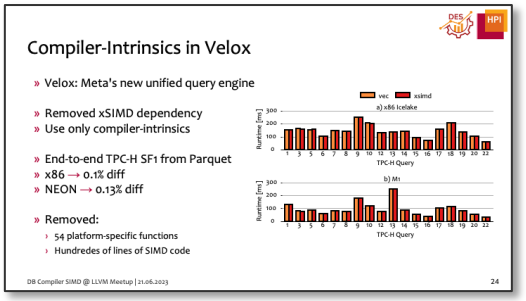
Summary



Writing platform-intrinsics code is hard and cumbersome



Compiler-intrinsics generic and cross-platform



Compiler-intrinsics achieve the same performance

https://github.com/hpides/autovec-db